

Curriculum Vitae : Kentaro Sano

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Dr. Kentaro Sano received his Ph.D. from the Graduate School of Information Sciences, Tohoku University, in 2000. Then he was a Research Associate at the Graduate School of Engineering in Stanford University, until 2001. Since 2001 until 2005, he had been a Research Associate at the Graduate School of Information Sciences, Tohoku University. Since 2005 until present, he has been an Associate Professor at the Graduate School of Information Sciences, Tohoku University. He was a visiting researcher at the Department of Computing in Imperial College, London since 2006 until 2007.

He has been a Program committee of IEEE conference series ASAP (Application-specific Systems, Architectures and Processors) since 2007 until present. He is a Program co-chair of International Workshop HEART (Highly-Efficient Accelerators and Reconfigurable Technologies) in 2010. He is a Member of IEEE (Institute of Electrical and Electronics Engineers) Computer Society, ACM (Association for Computing Machinery), IEICE (Institute of Electronics, Information and Communication Engineers) and PSJ (Information Processing Society of Japan).

His research interests are Reconfigurable Computing, Custom Computing Machines with FPGAs (Field-Programmable Gate Arrays), Accelerators for High-Performance Computing and Parallel Processing Architectures. In recent years, He has researched FPGA-based custom computing machines for high-performance floating-point computation including computational fluid dynamics, especially focusing on the custom structures for efficient data transfer and scalably expandable system.