

RESUME

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English Name Frank / Yu-Shen Cheng (Yeu-Shen Jehng)

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EDUCATION

Ph. D. of Electrical Engineering in National Taiwan University,
May 30 , 1992

Master of Electrical Engineering in National Taiwan University,
May 30 , 1989

Bachelor of Electrical Engineering in Chinese Culture University,
May 30, 1987

EXPERIENCE

(Mar. 2010 – till now)

富興科技有限公司

Fu Sing Technology Co. Ltd.

General Manager

www.fusingtech.com

(Aug. 2002 – Feb. 2010)

麗臺科技股份有限公司

Leadtek Research Inc.

Deputy Chief Engineer (副總工程師)

Head of SOC, Multi-core, and Video Codec R&D Department

(in charge of 6 SOC engineers and 6 software codec engineers)

Responsibilities:

1. GPU and CELL application system development
3. R&D team management
4. ARM SOC development for video application
5. Technical research of video SOC
6. Video DSP system design
7. Video Codec (H.264 and MPEG4) development

(Oct. 1999 – Aug. 2002)

德碩半導體科技股份有限公司

TECHSOFT TECHNOLOGY

ASIC Design Dept. Manager

Responsibilities:

1. Microprocessor chip integration
2. Technical research and training
3. Chip architecture development
4. Video Codec design for surveillance system
5. FPGA/CPLD emulation
6. Chip design flow control
7. Verilog coding and functional simulation
8. Gate level verification
9. Transistor level verification
10. Chip sign off
11. Final chip testing

(Oct. 1992 - Oct. 1999)

中山科學研究院

Department of Defense (R.O.C.)

CSIST (Chung-Shan Institute of Science and Technology)

Project leader of ASIC design center

- Responsibilities:
1. Define project Spec.
 2. Schedule control and job allocation
 3. Algorithm mapping to chip architecture
 4. Develop high performance chip architecture
 5. Chip performance analysis
 6. FPGA/CPLD emulation
 7. Chip design flow control
 8. Verilog coding and functional simulation
 9. Real time video system development
 10. Image processing system development

(Jan.-Aug.,1994)

In-Plant Representative to stay in UNISYS (Long Island, USA) and MARTIN MARIETTA (New Jersey) for military project

SKILLS

1. Development of CUDA massive parallel processing
2. CELL multi-core system development
3. WinCE and Linux embedded SOC system development
4. VHDL / Verilog RTL coding
5. High level chip synthesis, gate-level timing verification, and post layout timing verification
6. Systolic array processor design for parallel processing
7. Digital image processing
8. Digital Wavelet Transform for video/audio coding
9. Video compression (JPEG, JPEG2000, MPEG4, H.264 standards)
10. Digital signal processing (FFT and digital filter design)
11. CPLD and FPGA emulation (ALTERA and XILINX FPGA emulation)
12. High performance computer architecture design (RISC computer, microprocessor and DSP)
13. High speed VLIW DSP development
14. MATLAB programming for algorithmic development
15. C language programming
16. Assembly language programming

IMPLEMENTATIONS

1. **Embedded system development for video application**
(WinCE 6.0 and Linux)
2. **H.264 encoder chip development**
(30 D1 frames per second video compression,
Baseline profile,

Integer, half-pel, and quarter-pel motion estimation engine,
Macroblock partitioning,
Integer DCT, inverse DCT transform, and quantization,
Deblocking filter, RDO and rate control,
CAVLC)

3. 64-bit VLIW video DSP chip design

(4 high-precision MAC and 8 low-precision MAC architecture,
high efficient datapath architecture with multi-port memory,
ALTERA FPGA functional emulation,
TSMC 0.18um process implemented,
PLL frequency pump to work at 240 Mhz,
Verilog RTL coding,
NC-Verilog all level verification)

4. Digital Wavelet Transform chip design

(Integer lifting wavelet architecture,
Applied to JPEG2000 image/video compression,
EBCOT and Arithmetic coding architecture design,
Integration to ARM7 32-bit microprocessor,
VHDL RTL coding,
ModelSim and Verilog-XL functional simulation,
ALTERA FPGA functional emulation,
UMC 0.25um process implemented)

5. Security Surveillance chip design

(Pixel data capture from CMOS image sensors,
Image processing to the pixel data,
Scene change detection,
Alarm message signaling,
UMC 0.25um process implemented)

6. Single chip 8-bit microprocessor design

(RISC CPU, single cycle instruction execution,
instruction fetch and execution are pipelined,
power save mode, watch dog timer, dual counters, and LCD driver,
ALTERA CPLD FLEX10KA functional emulation,
SYNOPSIS Design Compiler synthesis with VHDL entry,
Verilog-XL gate-level timing verification after synthesis,
PrimeTime static timing analysis,
TimeMill whole chip transistor-level timing verification after
placement and route,
LG 0.5um process implemented)

7. USB device controller design

(Specification 1.1 compliant)
(SIE : Serial Interface Engine design,
Interface specification define between microprocessor and USB,
USB integration to microprocessor,

UMC 0.25um process implemented)

8. **Wireless Keyboard / Mouse / Earphone**
(TRF6900 RF controller ASIC design,
PS2 interface controller ASIC design)
9. **TMS320C40 DSP image multiprocessing system design**
(C40 single board computer with A/D, D/A, and RS-232 interfaces,
Four parallel processing boards in the system,
General purpose DSP computing system for algorithm realization,
infrared image processing algorithm develop,
laser radar scene matching algorithm develop,
RS-170 video data conversion,
ALTERA CPLD peripheral controller design)
10. **Single chip FFT processor design**
(Mixed radix 4/radix 2 FFT architecture,
1024 points processing capability,
Data paths: Wallace tree modified Booth multipliers,
Dual-bank memory modules for parallel data loading,
LSI logic CMDE sign off procedure,
LSI 0.5um process implemented)
11. **Motorola 68030 CPU board design for naval combat system**

TRAINING

1. TMS320C6x DSP technical training
2. FPGA EXPRESS for CPLD and FPGA synthesis
3. SYNOPSYS Design Compiler workshop
4. SYNOPSYS PrimeTime static timing analysis workshop
5. SYNOPSYS TimeMill mixed signal CMOS transistor-level timing simulation workshop
6. XILINX high density FPGA applications

Publication List

Yu-Shen Cheng / Yeu-Shen Jehng

(A) Refereed Paper (International Journal)

- [1] **Y. S. Jehng**, L. G. Chen, and T. M. Parng, "ASG: Automatic Schematic Generator", *INTEGRATION, the VLSI journal*, Vol. 11, No. 1, March 1991, pp.11-27.
- [2] L. G. Chen, W. T. Chen, **Y. S. Jehng**, and T. D. Chiueh, "An Efficient Parallel Motion Estimation Algorithm for Digital Image Processing". *IEEE Trans. on Circuits and Systems for Video Technology*, Vol 1, No.4, December 1991, pp.378-385.
- [3] T. H. Chen, L. G. Chen, and **Y. S. Jehng**, "Design and analysis of VLSI-based arithmetic arrays with error correction", *International Journal of Electronics*, Vol.72, No.2, April 1992, pp.253-271.
- [4] **Y. S. Jehng**, L. G. Chen, and T. D. Chiueh, "An Efficient and Simple VLSI Tree Architecture for Motion Estimation Algorithms". *IEEE Trans. on Signal Processing*, Vol 41, No.2, February 1993, pp.889-900.
- [5] **Y. S. Jehng**, L. G. Chen, and T. D. Chiueh, "A Motion Estimator for Low Bit-rate Video Codec". *IEEE Trans. On Consumer Electronics*, Vol 38, No.2, May 1992, pp.60-69.
- [6] L. G. Chen, **Y. S. Jehng**, and T. D. Chiueh, "Pipeline Interleaving Design for FIR, IIR, and FFT Array Processors". *Journal of VLSI Signal Processing*, 10, 275-293(1995).

(B) Conference Paper

1. International Conference (IC)

- [1] **Y. S. Jehng**, L. G. Chen, and T. D. Chiueh, "Low Latency Tree Architecture for Motion Estimation Algorithms", *IASTED International Symposium on Adaptive Control and Signal Processing*, New York, USA, Oct. 1990, pp.52-55.
- [2] **Y. S. Jehng**, L. G. Chen, T. D. Chiueh, W. T. Chen, and H. M. Jong, "Pipeline Interleaving Design for FIR, IIR, and FFT", *90-SASIMI Synthesis and Simulation Meeting and International Interchange*, Tokyo, Japan, Oct. 1990, pp.207-214.
- [3] L. G. Chen, **Y. S. Jehng**, and T. M. Parng, "Automatic Schematic Environment

for CAD Frameworks”, 1990 International Electronic Devices and Materials Symposium, Hsinchu, ROC, Nov. 1990, pp.502-505.

- [4] L. G. Chen, **Y. S. Jehng**, and T. D. Chiueh, “Array Architecture Design for Video Communication Applications”, Proc. Of International Computer Symposium, Hsinchu, R.O.C. Dec. 1990, pp.272-277. (**The Best Paper Award from R.O.C. Computer Society in 1990.**)
- [5] L. G. Chen, W. T. Chen, **Y. S. Jehng**, and T. D. Chiueh, “An Efficient Parallel Motion Estimation Algorithm for Digital Image Processing”, *IEEE 1991 International Conference on Circuits and Systems (ISCAS'91)*, Singapore, pp.670-673, June 1991.
- [6] L. G. Chen, W. T. Chen, **Y. S. Jehng**, and T. D. Chiueh, “A Predictive Parallel Motion Estimation Algorithm for Digital Image Processing”, *IEEE ICCD'91*, pp.617-620, Oct. 1991.
- [7] T. H. Chen, L. G. Chen, and **Y. S. Jehng**, “The chip design for fault-tolerant FFT processor”, *1991 International Symposium on Communications*, Tainan, December 1991.
- [8] T. H. Chen, L. G. Chen, and **Y. S. Jehng**, “A Partitioning approach to design fault-tolerant arithmetic arrays”, *1992 International Phoenix Conference on Computer and Communication (IPCCC'91)*, Arizona, pp. 432-439, April 1992.
- [9] **Y. S. Jehng** and L. G. Chen, “Realization of array architecture for video compression algorithms”, *1992 IEEE International Symposium on Circuits and Systems (ISCAS'92)*, San Diego, May 1992.
- [10] **Y. S. Jehng**, L. G. Chen, and T. D. Chiueh, “A motion estimator for low bit-rate video codec”, *1992 International Conference on Microwave and Communication (ICMC'92)*, Nanjing, June 1992.
- [11] **Y. S. Cheng** and Gen-Dow Huang, “Image and Audio Wavelet Integration for Home Security Video Compression”, *Proceedings of SPIE Wavelet and Independent Component Analysis Applications IX Conference*, Orlando, pp. 440-447, April 2002.
- [12] **Y. S. Cheng** and Gen-Dow Huang, “Audio/Video Compression Applications using Wavelets”, *2002 International Joint Conference on Neural Networks (IJCNN'02)*, Honolulu, May 2002.

2. Local Conference (LC)

- [1] L. G. Chen, **Y. S. Jehng**, and T. D. Chiueh, "VLSI Array Processor for Low Bit Rate Video System", *Proc. Of Telecommunication Symposium*, Hsinchu ROC, Dec. 1990, pp.311-316.
- [2] T. H. Chen, L. G. Chen, and **Y. S. Jehng**, "A cost-effective fault-tolerant design of VLSI-based arithmetic units using partitioning technique", *1991 National Computer Symposium (NCS)*, Chung-Li, pp.132-137, December 1991.

3. Workshop Presentation (WK)

- [1] **Y. S. Jehng**, L. G. Chen, and T. M. Parng, "ASG: Automatic Schematic Generator", *Proc. Of 2nd VLSI/CAD Workshop*, March 1990, Taiwan, ROC.
- [2] **Y. S. Jehng**, L. G. Chen, T. D. Chiueh, and T. H. Chen, "Realization of Array architectures for hierarchical block matching algorithms", *1992 IEEE International Workshop on Intelligent Signal Processing and Communication System: ISPACS*, Taipei, ROC, March, 1992, pp.368-378.

(C) Books (BK)

- [1] **Y. S. Jehng**, L. G. Chen, T. D. Chiueh, W. T. Chen, and H. M. Jong, "Pipeline Interleaving Design for FIR, IIR, and FFT", in Section: CAD for DSP of *VLSI Logic Synthesis and Design*, ISBN90-51990460, Edited by Robert W. Dutton, IOS Press, Netherlands, 1991.
- [2] **鄭羽仲** Verilog 數位電路設計-範例寶典(基礎篇) 儒林圖書 (TB028) 2006 年 9 月.